

1 1. A CMOS circuit fabricated using a process that can create thick oxide
2 transistors and thin oxide transistors, comprising:

3 a differential logic circuit fabricated of thin oxide transistors, and having a
4 plurality of inputs; and

5 a current source, supplying bias current to the differential logic circuit, the
6 current source fabricated using at least one thick oxide transistor.

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8 2. The apparatus according to claim 1, wherein the current source has a
9 control input that can determine how much current is available to source to the
10 differential logic circuit.

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12 3. The apparatus according to claim 2, further comprising an adaptive bias
13 control that provides a control signal at the control input of the current source to
14 increase the bias current available to the differential logic circuit.

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16 4. The apparatus according to claim 3, further comprising means for
17 selectively adjusting an amount of bias current available to the logic circuit.

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1 5. The apparatus according to claim 2, further comprising an adaptive bias
2 control, coupled to at least one of the logic inputs, and is responsive to a voltage
3 transition on the logic input to provide a control signal at the control input of the
4 current source to increase the bias current available to the differential logic
5 circuit.

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7 6. The apparatus according to claim 5, further comprising a bias load circuit
8 loading the differential logic circuit.

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10 7. The apparatus according to claim 6, wherein the bias load circuit has a
11 load current control input; and

12 wherein the adaptive bias control is responsive to the voltage transition on
13 the logic input to provide a load current control signal at the load current control
14 input of the bias load circuit to increase the bias current through the load.

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16 8. The apparatus according to claim 6, wherein the bias load circuit
17 comprises a resistive load.

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19 9. The apparatus according to claim 1, wherein the differential logic circuit
20 has a differential output voltage swing of less than 300mV.

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1 10. The apparatus according to claim 1, wherein the differential logic circuit
2 has a differential output voltage swing of between 100mV and 300mV.

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4 11. The apparatus according to claim 1, wherein the differential logic circuit
5 comprises a pair of matched thin oxide transistors configured as a differential
6 inverter.

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1 12. A CMOS circuit fabricated using a process that can create thick oxide
2 transistors and thin oxide transistors, comprising:

3 a differential logic circuit fabricated of thin oxide transistors, and having a
4 plurality of inputs;

5 a current source, supplying bias current to the differential logic circuit, the
6 current source fabricated using at least one thick oxide transistor, the current
7 source having a control input that can determine how much current is available to
8 source to the differential logic circuit; and

9 an adaptive bias control that provides a control signal at the control input
10 of the current source to selectively control the bias current available to the
11 differential logic circuit.

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13 13. The apparatus according to claim 12, wherein the adaptive bias control is
14 coupled to at least one of the logic inputs, and is responsive to a voltage
15 transition on the logic input provides a control signal at the control input of the
16 current source to control the bias current available to the differential logic circuit.

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18 14. The apparatus according to claim 12, further comprising a bias load circuit
19 loading the differential logic circuit.

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1 15. The apparatus according to claim 14, wherein the bias load circuit has a
2 load current control input; and

3 wherein the adaptive bias control is responsive to the voltage transition on
4 the logic input to provide a load current control signal at the load current control
5 input of the bias load circuit to control the bias current through the load.

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7 16. The apparatus according to claim 14, wherein the bias load circuit
8 comprises a resistive load.

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10 17. The apparatus according to claim 12, wherein the differential logic circuit
11 has a differential output voltage swing of less than 300mV.

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13 18. The apparatus according to claim 12, wherein the differential logic circuit
14 has a differential output voltage swing of between 100mV and 300mV.

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1 19. A CMOS circuit fabricated using a process that can create thick oxide
2 transistors and thin oxide transistors, comprising:

3 a differential logic circuit fabricated of thin oxide transistors, and having a
4 plurality of inputs, the differential logic circuit comprising a pair of matched thin
5 oxide transistors configured as a differential inverter;

6 a current source, supplying bias current to the differential logic circuit, the
7 current source comprising a thick oxide transistor receiving a supply voltage at a
8 drain thereof and coupling a reduced supply voltage to the differential logic circuit
9 through a source thereof, the current source having a control input at a gate
10 thereof that can determine how much current is available to source to the
11 differential logic circuit; and

12 an adaptive bias control that provides a control signal at the control input
13 of the current source to selectively control the bias current available to the
14 differential logic circuit.

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16 20. The apparatus according to claim 19, wherein the adaptive bias control is
17 coupled to at least one of the logic inputs, and is responsive to a voltage
18 transition on the logic inputs to provide a control signal at the control input of the
19 current source to control the bias current available to the differential logic circuit.

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21 21. The apparatus according to claim 19, further comprising a bias load circuit
22 loading the differential logic circuit.

1 22. The apparatus according to claim 21, wherein the bias load circuit has a
2 load current control input; and

3 wherein the adaptive bias control is responsive to the voltage transition on
4 the logic input to provide a load current control signal at the load current control
5 input of the bias load circuit to control the bias current through the load.

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7 23. The apparatus according to claim 19, wherein the bias load circuit
8 comprises a resistive load.

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10 24. The apparatus according to claim 19, wherein the differential logic circuit
11 has a differential output voltage swing of less than 300mV.

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13 25. The apparatus according to claim 19, wherein the differential logic circuit
14 has a differential output voltage swing of between 100mV and 300mV.

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